

Appl. No: 09/943,242
Amdt. Dated: March 22, 2005
Reply to Office action of December 22, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1(Currently Amended). A computing system comprising:
a processor having a data/control bus interface;
a data/control bus implementing one or more device communication
channels;
5 a data memory coupled to the processor;
a mass storage device having an interface for communicating mass
storage transactions; and
a controller having a memory interface coupled directly to the data
memory and a mass storage interface coupled directly to the mass storage
10 device's interface and operable to conduct mass storage transactions between
the data memory and the mass storage device.

2(Original). The computing system of claim 1 wherein the data memory
is coupled to the processor by a memory bus operating independent of the
data/control bus.

3(Original). The computing system of claim 2 wherein the controller
comprises a memory access controller coupled to the processor, the data
memory, and the mass storage device and operable to arbitrate accesses to the
data memory between the mass storage and the processor.

4(Original). The computing system of claim 2 wherein the controller
comprises a direct memory access controller coupled to the data/control bus,
wherein the mass storage interface comprises a logical connection formed using
one of the device communication channels.

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5(Original). The computing system of claim 1 wherein the data memory is coupled to the data/control bus.

6(Original). The computing system of claim 5 wherein the controller comprises a direct memory access controller coupled to the data/control bus and the memory interface comprises a logical connection formed using one of the device communication channels.

7(Original). The computing system of claim 1 further comprising storage controller processes and application behavior processes implemented using the processor.

8(Original). The computing system of claim 7 wherein the storage controller processes map storage requests generated by the application behavior processes expressed in logical geometry terms into storage requests expressed in physical geometry terms.

9(Original). The computing system of claim 1 wherein the data memory includes logic that map storage requests generated by the processor expressed in logical geometry terms into storage requests expressed in physical geometry terms.

10(Original). The computing system of claim 1 wherein the processor implements data structures storing physical geometry information about the mass storage device.

11(Original). The computing system of claim 1 wherein the data/control bus comprises at least one direct memory access (DMA) channel.

12(Original). The computing system of claim 1 wherein the controller is integrated with the processor on a single integrated circuit chip.

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13(Original). The computing system of claim 1 wherein the mass storage device's interface comprises a peripheral component interconnect (PCI) standard-compliant interface.

14(Original). The computing system of claim 1 wherein the mass storage device's interface comprises a small computer systems interface (SCSI) standard-compliant interface.

15(Original). The computing system of claim 1 wherein the mass storage device's interface comprises a universal serial bus (USB) standard-compliant interface.

16(Original). The computing system of claim 1 wherein the mass storage device's interface comprises an IEEE 1394 standard-compliant interface.

17(Original). The computing system of claim 1 wherein the mass storage device comprises:

a spinning disk having magnetic storage media provided on at least one surface;

5 a head for accessing data stored in the magnetic storage media;

an actuator mechanism for moving the head relative to the magnetic storage media in response to commands;

a servo controller coupled to receive requests transferred from the data memory by the controller and generate the commands to the actuator mechanism.
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18(Original). The computing system of claim 17 wherein the mass storage device's interface is implemented by the servo controller and implements a physical interface to the data/control bus and a physical interface to the head and actuator mechanism.

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5 19(Previously Presented). The computing system of claim 1 wherein the computing device comprises a set-top box including processes for implementing audio/video behaviors in the processor.

20(Previously Presented). The computing system of claim 1 wherein the computing device comprises a network appliance having a network controller coupled to the data/control bus.

21(Previously Presented). The computing system of claim 1 wherein the mass storage device comprises an optical storage device.

22(Previously Presented). The computing system of claim 1 wherein the mass storage device comprises a magneto-optical storage device.

Claims 23-31(Cancelled).